REMARKS

Claims 1, 3, 5, 6, 8, and 10 are all the claims pending in the application. By this Amendment, Applicant amends claims 1, 5, 6, and 8 to further clarify the invention. Moreover, Applicant adds claim 10. Claim 10 is clearly supported throughout the specification.

Claim Rejections under 35 U.S.C. § 112

The Examiner rejected claims 1, 3, and 5 under section 112, second paragraph. Applicant thanks the Examiner for pointing out, with particularity, the aspects of the claims thought to be indefinite. Applicant respectfully requests the Examiner to withdraw this rejection of claims 1, 3, and 5 in view of the self-explanatory claim amendments being made herein.

Claim Rejections under 35 U.S.C. § 103

With regard to the prior art rejection, the Examiner maintained the rejection of claims 1, 3, 5, 6, and 8 under 35 U.S.C. § 103(a) as being unpatentable over Applicant's admitted prior art (hereinafter "APA") in view of Japanese Patent Publication No. 01-173149 to Oshikawa (hereinafter "Oshikawa"). Applicant respectfully traverses this rejection in view of the following comments.

In the exemplary, non-limiting embodiment of the present invention, a data transmission system is described that can execute continuous data transmission using fewer signal lines and without malfunctions caused by the disturbances between the control signals in the data transmission. The data transmission between the primary board and the secondary boards uses the same data transmission signal line as an address bus and a data bus, mutually. In particular, in the exemplary, non-limiting embodiment, the next transmission address is obtained by incrementing the transmission start address stored in the secondary board; therefore, there is no

need to read/write addresses every transmission operation. Accordingly, the continuous transmission can be accomplished using few signal lines.

Moreover, in this exemplary, non-limiting embodiment, a cycle signal that counts three times the leading edge of the clock to toggle is provided. That is, the secondary board does not shift to the next process until the phase has been toggled. The leading and trailing edges of the trigger detected in combination with the toggle states of the phase prevents disturbances generated on the trigger. This exemplary embodiment is provided by way of an example only and is not intended to limit the scope of the claims in any way.

Oshikawa teaches performing the transfer of data at a high speed by producing automatically a series of addresses which are necessary for accesses to all access areas desired by an application module within a memory module based on the head address of a relevant area.

Specifically, Oshikawa teaches an address buffer containing a counter function which is used together with a bus interface which controls a swap means. Then a series of addresses which are necessary for accesses to all access areas are successively produced by the buffer 44 under the control of the interface. An application module is not required to deliver said series of addresses after the output of the head address of a desired access area and therefore can use an address/data line only for transfer of the read data. As a result, data can be transferred at a high speed compared with a conventional case where the address/data line is used alternately for transfer of the read address received from the application module and the data received from a memory module.

Of the rejected claims, only claims 1, 5, 6, and 8 are independent. The Examiner contends that APA and Oshikawa suggest each feature of the independent claims. The Examiner

acknowledges that APA does not teach or suggest generating an address, where the cycle signal indicating the switching of data is used in combination with the trigger signal (see pages 4-6 of the Office Action).

In particular, the Examiner acknowledges that APA does not teach or suggest "wherein an address used in the data access in the secondary boards is generated based on the start address, a predetermined trigger signal and a cycle signal indicating switching of data, the cycle signal is combined with the trigger," as recited in claim 1, "address is generated... wherein a cycle signal indicating switching of data is used in combination with a trigger signal," as recited in claim 5, "informs a trigger signal combined with a cycle signal indicating a timing of data access, and a start address required for data read via the data transmission path,...increments the start address at a timing of the trigger signal," as recited in claim 6, and "informing a trigger signal combined with a cycle signal indicating a timing of data access and a start address required for data write via the data transmission path,... incrementing the start address at a timing of the trigger signal," as recited in claim 8.

The Examiner alleges that Oshikawa cures the deficient teachings of the APA. The Examiner alleges that Oshikawa teaches having a cycle signal in combination with the trigger signal that would indicate the switching to the previous data while alternating L/H for each switching of data. Specifically, the Examiner alleges that the data enable signal 68 is used in combination with the counter signal 71 that would indicate the switching to the previous data while alternating L/H for each switch of data cycle signal, *i.e.*, switching of D_{4A}...on the Address/Data line 52 is indicated by a combined signal of the counter signal, low pulse signal, then the data enable signal, high pulse (see pages 3-4 and 10 of the Office Action). Applicant

respectfully disagrees. Applicant has carefully studied Oshikawa's teachings of the high pulse (data enable signal) and low pulse (counter signal), which are not similar to having a cycle signal that would indicate the switching of data and having this cycle signal be combined with the trigger signal.

Oshikawa only teaches using the data enable signal 68 and the counter signal 71 to increment an address (D_{4A}, D_{4A+1}, D_{4A+2},...), *e.g.*, Fig. 2. However, in Oshikawa, there is no teaching or suggestion that the two signals are used in combination. That is, in Oshikawa, there is no cycle signal that would indicate the switching of data by H/L alternate. In other words, Oshikawa fails to teach or suggest having this cycle signal that indicates the switching of data by H/L alternate being used in combination with the trigger.

Oshikawa's data enable signal 68b and counter signal 71 do not prevent the address from being erroneously incremented due to the deformation of the wave of the count signal during data enabling, which is caused by external noise or signal reflection. In other words, Oshikawa fails to teach or suggest not incrementing or generating an address during the time in which the waveform is deformed by the count signal or noise. In short, Oshikawa fails to teach or suggest generating an address based on the trigger signal combined with a cycle signal that indicates switching of data. Oshikawa does not cure the deficient teachings of the APA.

Therefore, "wherein an address used in the data access in the secondary boards is generated based on the start address, a predetermined trigger signal and a cycle signal indicating switching of data, the cycle signal is combined with the trigger," as set forth in claim 1, "address is generated... wherein a cycle signal indicating switching of data is used in combination with a trigger signal," as set forth in claim 5, "informs a trigger signal combined with a cycle signal

indicating a timing of data access, and a start address required for data read via the data transmission path,...increments the start address at a timing of the trigger signal," as set forth in claim 6, and "informing a trigger signal combined with a cycle signal indicating a timing of data access and a start address required for data write via the data transmission path,... incrementing the start address at a timing of the trigger signal," as recited in claim 8, is not suggested or taught by the combined teachings of APA and Oshikawa, which lack generating or incrementing an address based on a trigger signal combined with a cycle signal that indicates the switching of data.

For at least these exemplary reasons, Applicant respectfully requests the Examiner to carefully reconsider and to withdraw this rejection of claims 1, 5, 6, and 8. Claim 3 is patentable at least by virtue of its dependency on claim 1.

New Claim

In order to provide more varied protection, Applicant adds claim 10. Claim 10 is patentable at least by virtue of its recitation of "informing a trigger signal combined with a cycle signal indicating a timing of data access and a start address required for data write via the data transmission path."

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly invited to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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